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Code No: 124CN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, December - 2024 /January - 2025

COMPUTER ORGANIZATION

(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART- A

(25 Marks)

1.a)	Write a short note on I/O units.	[2]
b)	What is the purpose of status bit conditions?	[3]
c)	Define the term "synchronous data transfer".	[2]
d)	List the benefits of isolated I/O.	[3]
e)	Define virtual memory.	[2]
f)	Differentiate between RAM and ROM.	[3]
g)	List the general purpose registers in 8086.	[2]
h)	What is the purpose of the segment registers in the 8086 CPU?	[3]
i)	Define an assembly language program.	[2]
j)	Write the syntax for a JMP instruction.	[3]

PART-B

(50 Marks)

2.a) Evaluate the impact of different addressing modes on the efficiency of instruction execution.
b) Explain the purpose and types of program interrupts. [5+5]

OR

3. Describe the concept of addressing modes in computer architecture. Outline different addressing modes with examples to show how they impact instruction execution. [10]

4.a) Demonstrate the operation of asynchronous data transfer using strobe control, and outline its typical use cases.
b) Outline the difference between an I/O bus and a memory bus. [6+4]

OR

5. Explain the following.
a) Modes of transfer.
b) IOP-CPU-IOP Communication. [5+5]

6.a) Outline the process of creating a memory address map.
b) Justify the use of cache memory in CPUs by evaluating its benefits and potential drawbacks. [5+5]

OR

7.a) Differentiate between associative and set associative mapping.
b) Determine miss and hit ratio in cache systems. [5+5]

8. Demonstrate the structure and purpose of the 8086 pin diagram with a detailed diagram and explanation of each pin. [10]

OR

9.a) Explain how pipelining enhances performance and discuss any limitations.
b) Illustrate the structure and functionality of the 8086 flag register. [4+6]

10. Determine the role of branch instructions in assembly language control flow, and demonstrate their usage with examples. [10]

OR

11.a) Describe the process of evaluating an arithmetic expression in 8086.
b) Illustrate the syntax and functionality of CALL and RET instructions. [5+5]

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